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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,629	11/17/2003	Frederic Boutaud	7020	4322

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EXAMINER	
LAI, VINCENT	
ART UNIT	**PAPER NUMBER**
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,629	BOUTAUD, FREDERIC	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5* is/are allowed.

6)☒ Claim(s) *6-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 3/2/2005 was considered by the examiner.

Response to Arguments

2. In view of the Appeal Brief filed on 16 January 2007, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

3. Applicant's arguments filed 16 January 2007 have been fully considered but they are not fully persuasive.

With regard to claim 6, Applicant argues on page 13 of the Appeal Brief, "Examiner alleges that Morley discloses accessing the unified memory a first time during the second instruction cycle with a dummy access when it is determined that the program instruction accessed for a second instruction cycle is a conditional program code discontinuity." The Applicant further elaborates argument and concludes on page 14, "In other words, Morley fails to discuss or disclose any type of dummy access of the unified memory."

It is to be noted that in the last paragraph of page 8 in the Applicant's Specification, a dummy access is taught as being an instruction commands that performs an update. Morley teaches a dummy access in figure 28 and column 58, lines 17-20. During phase phi, updates are done during a fetch. The language of the cited lines clearly states that memory is read/written to and updates occur during phase phi.

Applicant argues on page 14 and continuing onto page 15, "Examiner alleges that Morley discloses accessing the unified memory a second time during the second instruction cycle to read a new instruction when it is determined the program instruction accessed for a second instruction cycle is a condition program code discontinuity...with respect to Figure 28 the read operation [in Morley] illustrates that during the [phi] of the

MIO cycle, the data from the memory is accessed...thus the memory is only access once per MIO cycle."

Applicant readily acknowledges at least one memory access is made. Examiner believes the above explanation of the dummy access rectifies this disagreement, in which the dummy access is the first access and the acknowledged memory access is the second one.

The arguments of claim 9, found on pages 15-17, mirror that of the arguments above and thus such explanation are meant to also apply to the arguments of claim 9.

The argument of claims 10 and 11, found on pages 17-19, are directly contingent on the argument of claim 9 and thus are rectified with the rectification of claim 9.

The arguments of claim 13, found on pages 19-21, mirror that of the arguments above and thus such explanation are meant to also apply to the arguments of claim 9.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Morley (U.S. Patent # 4;276,594), herein referred to as Morley.

As per **claim 6**, Morley discloses a method for accessing a unified memory in a micro-processing system having a microprocessor, a one level pipeline, and a two-phase clock, such that an instruction is executed in a single instruction cycle, comprising:

(a) fetching (See figure 19, and column 18, lines 33-40: A fetch must be done) a program instruction, corresponding to a second instruction cycle, from the unified memory (Public Memory 33, see figure 5) during a first instruction cycle;

(b) determining if the fetched program instruction corresponding to the a second instruction cycle is a conditional program code discontinuity (See column 1, lines 32-36: A decision is made to what sort of instruction was fetched);

(c) accessing the unified memory a first time during the second instruction cycle with a dummy access (See column 58, lines 17-20: During phase phi, updates are done during a fetch, which is what happens when a dummy access is executed) when it is determined that the fetched program instruction corresponding to the second instruction cycle is a conditional program code discontinuity; and

(d) accessing the unified memory a second time (See figure 28: On a read, there is two reads done) during the second instruction cycle to read a new instruction when it is determined the fetched program instruction corresponding to the second instruction cycle is a conditional program code discontinuity, thereby delaying instruction access

from the unified memory for the second instruction cycle by a half cycle (See figure 19: There is a phase gap between reads).

As per **claim 7**, Morley discloses wherein the conditional program code discontinuity is a jump instruction (See column 39, lines 3-7: Jump is a special instruction).

As per **claim 8**, Morley discloses wherein the conditional program code discontinuity is a call instruction (See column 36, lines 43-46: Call instructions are handled differently from other instructions).

As per **claim 9**, Morley discloses a method for accessing a unified memory in a micro-processing system having a microprocessor, a one level pipeline, and a two-phase clock, such that an instruction is executed in a single instruction cycle, comprising:

(a) fetching (See figure 19, and column 18, lines 33-40: A fetch must be done) a program instruction from the unified memory (Public Memory 33, see figure 5);

(b) determining (See column 1, lines 32-36: A decision is made to what sort of instruction was fetched) if the fetched program instruction is a loop initiation instruction;

(c) storing (See column 46, table 14: Op code is stored in an instruction register) a first instruction of the loop in an instruction register when the fetched program instruction is a loop initiation instruction;

(d) executing the loop (See column 41, line 67-column 42, line 1: Loops are executed with a special case for single instruction loops);

(e) determining if a fetched instruction during the execution of the loop is a last instruction of the loop (See column 1, lines 32-36: A decision is made to what sort of instruction was fetched);

(f) accessing the unified memory a first time, during the instruction cycle associated with the fetched last instruction of the loop, with a dummy access (See column 58, lines 17-20: During phase phi, updates are done during a fetch, which is what happens when a dummy access is executed);

(g) fetching the first instruction of the loop from the instruction register (See figure 19, and column 18, lines 33-40: A fetch must be done), during the instruction cycle associated with the fetched last instruction of the loop; and

(h) accessing the unified memory a second time, during the instruction cycle associated with the fetched last instruction of the loop, with a data access (See figure 28: On a read, there is two reads done).

As per **claim 10**, Morley discloses wherein the data access is a read data access (See figure 28: Read is one data access operation).

As per **claim 11**, Morley discloses wherein the data access is a write data access (See figure 28: Write is one data access operation).

As per **claim 12**, Morley discloses wherein the instruction register is an instruction stack (See column 36, lines 43-46: Call instructions are placed in a stack), thereby enabling program instruction fetches for nested loops (See column 18, lines 33-39: Fetching of a nest of code (which can be a nested loop) is allowed).

As per **claim 13**, Morley discloses a method for accessing a unified memory in a micro-processing system during execution of a loop instruction, comprising:

(a) accessing (See figure 19, and column 18, lines 33-40: A fetch must be done, which accesses the memory) a program instruction from the unified memory (Public Memory 33, see figure 5) during a first instruction cycle;

(b) determining a type of program instruction (See column 1, lines 32-36: A decision is made to what sort of instruction was fetched);

(c) pre-fetching a second instruction from the unified memory (See figure 28: On a read there is two reads done, the second read being possible to be a pre-fetch);

(d) saving the pre-fetched instruction in a register when it is determined that the type of program instruction is a first instruction of a loop (See column 46, table 14: Op code is stored in an instruction register);

(e) fetching an instruction from the register (See column 46, table 14: Op code is read from an instruction register) when it is determined that the type of program instruction is a last instruction of a loop;

(f) accessing the unified memory with a dummy access (See column 58, lines 17-20: During phase phi, updates are done during a fetch, which is what happens when a dummy access is executed) during execution of the last instruction of the loop; and

(g) accessing the unified memory, a second time, with a data access during execution of the last instruction of the loop (See figure 28: On a read, there is two reads done).

As per **claim 14**, Morley discloses wherein the pre-fetched instruction is saved in a stack (See column 36, lines 43-46: Call instructions are placed in a stack) when it is determined (See column 1, lines 32-36: A decision is made to what sort of instruction was fetched) that the type of program instruction is first instruction of a loop to enable nested loops and interruptible loops, and a next instruction is fetched from the stack (See column 46, table 14: Op code is read from an instruction register) when it is determined that the type of program instruction is a last instruction of the loop.

Allowable Subject Matter

5. Claims 1-5 are allowed.

The primary reasons for allowance of claim 1 in the instant application rest at least in the combination with the inclusion of the limitation that "a method of accessing a unified memory in a microprocessing system...such that an instruction is executed in a single instruction cycle, comprising...determining if the fetched program instruction

would require three unified memory accesses during a single instruction cycle for proper execution of the fetched program instruction." The prior art of record neither anticipates nor renders obvious the above-recited combination.

Because claims 2-5 depend directly or indirectly on claim 1, these claims are considered allowable for at least the same reasons noted above with respect to claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Lai
Examiner
Art Unit 2181

May 29, 2007
vl

DONALD SPARKS
SUPERVISORY PATENT EXAMINER